Application Paper

Fruit Inspection Application

The following outlines a real-time fruit inspection application. To measure the quality of fruit, the colors and shapes are used. The fruit is imaged with a color digital imaging system, the images are analyzed, and results reported to a host computer to determine the final disposition of each piece of fruit. The fruit is presented to the imaging system at a rate of 10 per second. It is a design requirement that all the fruit be inspected.

Application Steps

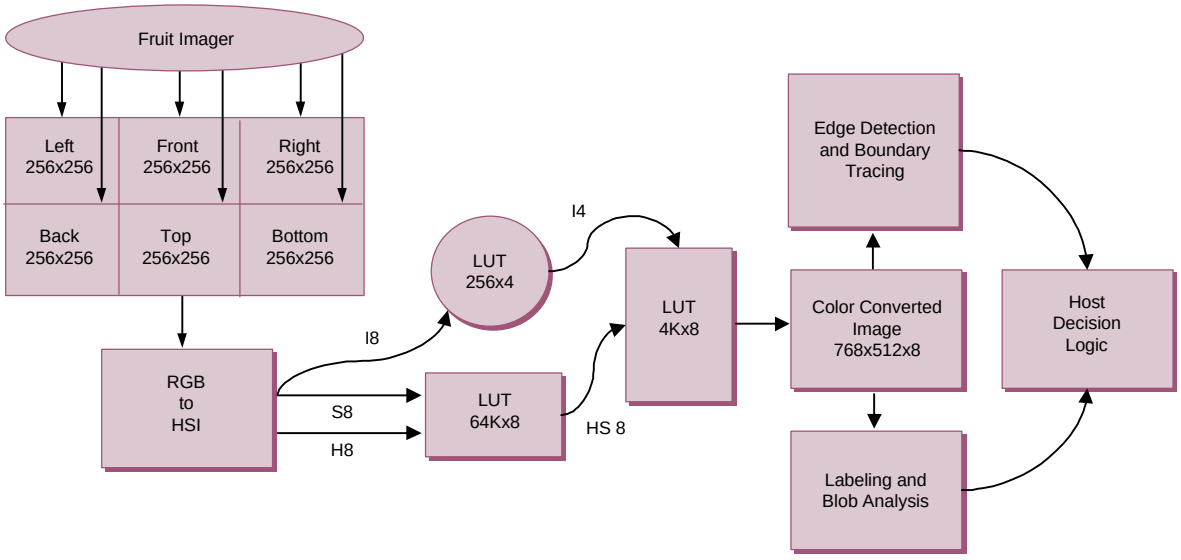
Collecting the Image

During this phase of the application the fruit is imaged by a camera that captures the fruit from six directions – front, left, back, right, top, and bottom – and supplies these images to the computer system as six separate images, each at 256x256 pixels. The six images are merged into one image of 768x512 for ease of handling, three images across and two down. This image is digitized as 24-bit RGB data.

Color Evaluation

The image is color space converted from RGB to HSI (hue, saturation and intensity). The three 8-bit values are converted to one 8-bit value by converting the 'I' value to a 4-bit value via a LUT (look up table), taking the H and S values and converting them to an 8-bit value via another LUT. The 12-bit value formed from the 4-bit intensity value and the 8-bit color value is converted to an 8-bit value via a final LUT. (In principle this could be done with one LUT of 16 MB deep.)

The values in the LUTs are precomputed to allow the color differences in the fruit that are significant to its grading to be easily detected. After the RGB pixel values are converted to the 8-bit pixels, a blob analysis is run on the image. Regions of constant color (8-bit value) are labeled in each of the 6 views. A table of regions is reported to the host computer containing the location of the blob, its size, color and bounding box. These values are used by the host computer to determine if the fruit is ripe, over-ripe, or damaged.



Real-time inspection system for fruit

Shape Evaluation

Shape evaluation is performed in each view by determining the perimeter of the fruit in each view, the area enclosed by the perimeter, the convex hull of the perimeter, and the area enclosed by the convex hull. The host computer uses the convex hull and the perimeter to determine if a piece of the fruit is missing or if the fruit is oddly shaped. For example, in the case of spherical fruit, the area of the convex hull and the perimeter should be nearly the same. However, for a banana, the convex hull will enclose more area than the perimeter.

Computational and Bus Band-width Requirements

The table below shows the counts of the number of operations and usage of memory for the TriMedia processor. Other processors have very similar counts with some small change in the I/O counts depending on how each vendor handles the I/O. These numbers are used to calculate the number of processors required, by computing the time it would take one processor to do the processing, and dividing that by the time actually available. This assumes that adding CPUs does not effect performance negatively, which is not true in a cluster design, but is true in a private memory design.

A simple way to implement the parallelism would be to assign one fruit-image set to each processor in rotation. This solution will keep up with the data rate, but does not provide the best latency, the time to compute the result for a given piece of fruit. If short latency is required the much more difficult problem of splitting a data set across multiple processors will have to be solved.

Operations	CPU Ops	BUS Bytes-R	BUS Bytes-W	I/O Bytes
Acquire front			786,000	786,000
Acquire left			786,000	786,000
Acquire back			786,000	786,000
Acquire right			786,000	786,000
Acquire top			786,000	786,000
Acquire bottom			786,000	786,000
Calibration		4,718,000		
Stitch image together	4,718,000		1,179,000	
Convert from RGB to HSI	17,694,000	1,179,000		
Convert HSI to color index	7,077,000		393,000	
Blob analysis	524,000	786,000	786,000	
Inspect Shape	866,000	430,000	720	720
Report enclosed area	786,000	393,000	240	240
Report perimeter length	64,000	21,000	240	240
Report convex hull area	15,000	15,000	240	240
Entire Application	30,881,000	7,114,000	7,078,000	4,719,000

Fruit Inspection Operation Counts

Processor Types

The performance of four popular microprocessors is considered in this application: the TriMedia TM1100 from Philips, the TMS320C6701 from Texas instruments, the ADSP21160 and ADSP21060 from Analog Devices. All of the processors support floating point and the table below indicates the significant difference between these processors.

Specification	Phillips TM1100	TI C6701	ADI 21160	ADI 20160
Architecture	VLIW	VLIW	VLIW	VLIW
FPU	yes	yes	yes	yes
MFLOPs (Peak)	665	1000	600	150
16x16 MACs (MMAC/s)	266	334	200	150
8x8 MACs (MMAC/s)	1064	334	200	150
MIPS (Peak)	665	1336	100	50
MOPS (Peak)	2500	1336	800	150
Memory Bus Bandwidth (MB/s)	400	332	400	160
1K FP cfft (µsec)	144	108	90	408
1K 16 bit cfft (µsec)	86	108	90	408
1K FP dot product (µsec)	3.85	3.07	5.12	26.6
1K 16 bit dot product (µsec)	1.9	3.07	5.32	26.6
512^2xFP Conv3x3 (msec)	8.87	7.11	11.80	47.19
512^2x8 bit Conv3x3 (msec)	4.43	7.11	11.80	47.19
512^2x8 bit Erosion/Dilation (msec)	1.11	1.77	3.93	15.73
"Glue" Logic Cost ($/CPU)	$ 3	$ 65	$ 39	$ 22
CPU Price ($)	$ 80	$ 150	$ 100	$ 270
# CPU for CT Rendering	3	3	3	13
# CPU for Inspection Example	2	3	2	8

VLIW Processor Comparison

Performance Comparison

The table above also delineates the number of processors needed to perform the specific application which was computed from quoted performance for algorithms from the various vendors or by instruction and memory access counts if the particular algorithm has not been reported by the processor vendor. When instruction and memory cycles are considered, it is assumed that the code has been optimized to obtain 80% of the theoretical maximum performance quoted by the vendor. The inspection and sorting application is limited by the bus bandwidth available and not by the computations being done. As a result a private memory design such as those found in Alacron's products, and most products using the TI TMS320C6700 scale well, as adding more processors increases the total memory bus bandwidth available to solving the problem.

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