



## ***FASTSERIES***

FAST4/1300 HARDWARE  
USER'S MANUAL

***FAST*** CAPTURE  
***FAST*** PROCESSING  
***FAST*** RESULTS

***FASTSERIES*** PCI BOARD

FastVision  
FastImage 1300  
FastFrame 1300

***FAST SERIES*** PMC

FastMem  
Fast4 1300  
Fast I/O 1300

30002-00180

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# **TABLE OF CONTENTS**

Copyright Notice .....	ii
Table of Contents .....	iii
Manual Figures & Tables .....	iv
Other Alacron Manuals .....	v
<b><i>I. INTRODUCTION</i></b> .....	<b>1</b>
<b>A. Fast4/1300</b> .....	<b>1</b>
<b>B. Components</b> .....	<b>1</b>
<b>C. Processor and Memory</b> .....	<b>1</b>
<b><i>II. FUNCTIONAL DESCRIPTION</i></b> .....	<b>2</b>
<b>A. Processors and Memory</b> .....	<b>2</b>
1. TriMedia Processors .....	2
2. Video Data Paths .....	3
3. Interrupts.....	3
4. Interprocessor Communication .....	4
<b>B. Digital Crosspoint Switch</b> .....	<b>5</b>
<b>C. PCI-PCI Bridge</b> .....	<b>5</b>
<b>D. Power</b> .....	<b>5</b>
<b><i>III. CONNECTOR</i></b> .....	<b>6</b>
<b>A. PMC (Pn1, Pn2, Pn4)</b> .....	<b>6</b>
<b><i>IV. SPECIFICATIONS</i></b> .....	<b>7</b>
<b>A. Processors</b> .....	<b>7</b>
<b><i>V. TROUBLESHOOTING</i></b> .....	<b>8</b>
<b><i>VI. ALACRON TECHNICAL SUPPORT</i></b> .....	<b>9</b>
<b>A. Contacting Technical Support</b> .....	<b>9</b>
<b>B. Returning Products for Repair or Replacements</b> .....	<b>10</b>
<b>C. Reporting Bugs</b> .....	<b>11</b>

## **MANUAL FIGURES & TABLES**

FIGURE	PAGE	SUBJECT	TABLE	PAGE	SUBJECT
1	1	Block Diagram of the Fast4/1300	1	6	PMC-Pn4 FastChannel Connectors
2	2	Processors and Memory			
3	4	TriMedia Interrupts			
4	4	Message Passing Connectors			

## **OTHER ALACRON MANUALS**

Alacron manuals cover all aspects of FastSeries hardware and software installation and operation. Call Alacron at 603-891-2750 and ask for the appropriate manuals from the list below if they did not come in your FastSeries shipment.

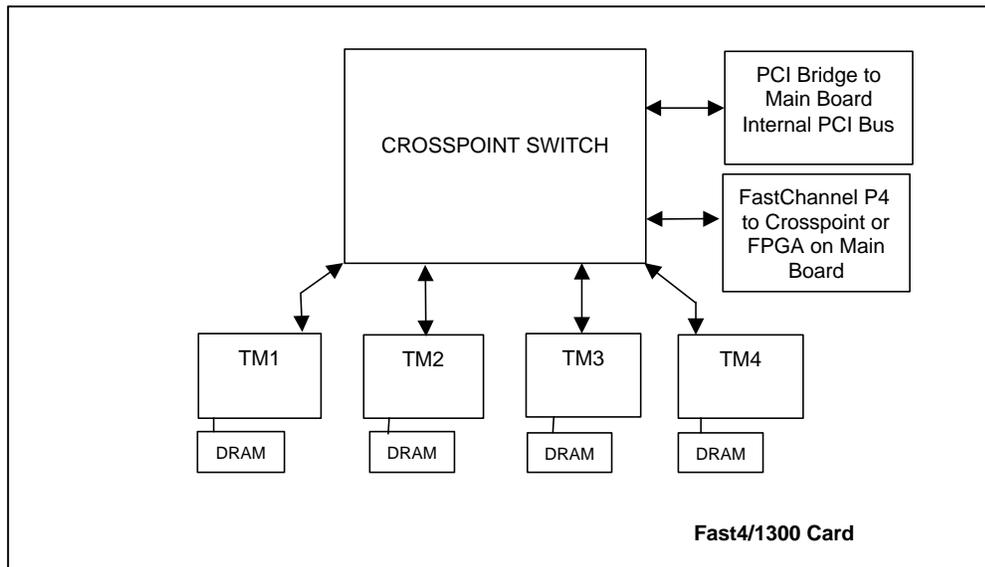
- 30002-00148 ALFAST Runtime Software Programmer's Guide & Reference
- 30002-00150 FastSeries Library User's Manual
- 30002-00153 Fast I/O Hardware User's Manual
- 30002-00155 FastMem Hardware User's Manual
- 30002-00162 FOIL – FastSeries **O**bject **I**maging **L**ibrary User's Manual
- 30002-00169 ALRT Runtime Software Programmer's Guide & Reference
- 30002-00170 ALRT, ALFAST & FASTLIB Software Installation Manual for Linux
- 30002-00171 ALRT, ALFAST, & FASTLIB Software Installation for Windows NT
- 30002-00172 FastImage 1300 Hardware User's Manual
- 30002-00173 FastMem Programmer's Guide & Reference
- 30002-00183 FastImage 1300 Camera Intergration User's Manual
- 30002-00184 FastSeries Getting Started Manual
- 30002-00185 FastVision Hardware Installation Manual
- 30002-00186 FastVision Software Installation Manual
- 30002-00187 FastFrame 1300 Hardware User's Manual



## **I. INTRODUCTION**

### **A. Fast4/1300**

The Alacron Fast4/1300 is a PMC daughter card module that can extend the processing power of an Alacron FastImage or FastFrame board by adding up to four TriMedia TM1300 processors and associated memory.



**Figure 1. Block Diagram of the Fast4/1300**

### **B. Components**

The Fast4/1300 includes the following components:

- PCI Bridge
- Crosspoint switch
- Cable for external 5V supply

### **C. Processor and Memory**

The Fast4/1300 can be configured with:

- One to four TriMedia TM1300 DSP processors
- 8MB or 16MB of SDRAM for each processor (all TMs on a card must have the same amount of SDRAM).

## II. FUNCTIONAL DESCRIPTION

### A. Processors and Memory

The processors and memory subsystem is diagrammed in Figure 2.

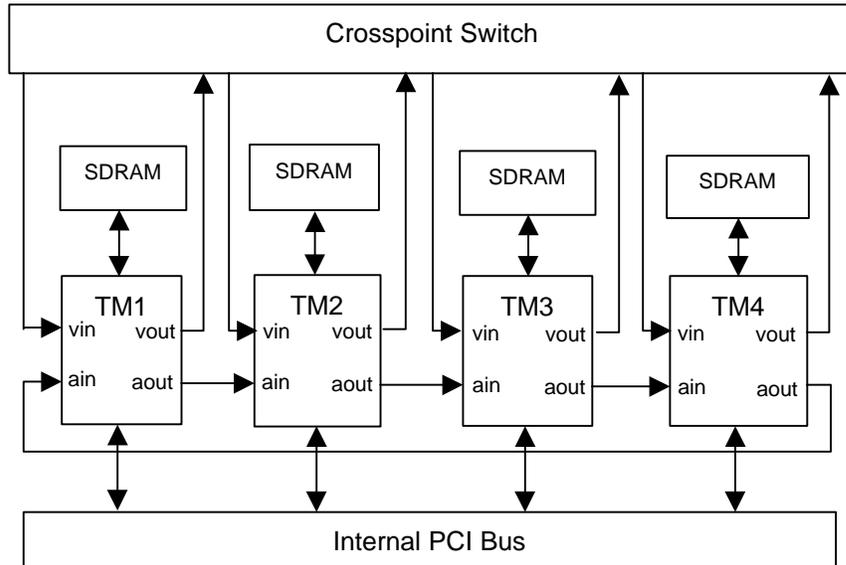


Figure 2. Processors and Memory

#### 1. TriMedia Processors

One to four TriMedia processors may be installed on the Fast4/1300 card. Processor TM1 is always installed; processors TM2, TM3, and TM4 are optional. These are 180 MHz or 200 MHz TM1300s. They have built-in PCI bus interfaces and glueless interface to 8 or 16 MB of local Synchronous Dynamic Random-Access Memory (SDRAM) for program and data.

The heart of the TriMedia is a VLIW digital signal processor which can issue up to 5 instructions in a single clock cycle for 900 peak MIPS (@ 180 MHz). Special DSP instructions allow simultaneous operation on four 8-bit or two 16-bit operands in a single instruction. This pushes the peak rate to over 2 billion operations per second for 8-bit data.

The TriMedia can issue up to four floating point operations per clock cycle for a peak rate of 720 MFLOPS. The TriMedia does not have floating point multiply/accumulate instructions, but it can issue up to two floating point adds and two floating point multiplies in a single clock cycle.

Each TriMedia has 8 or 16 megabytes of local SDRAM running at 143 MHz. The SDRAM is accessible from the host PCI bus (via the bridge) to allow the host to download programs, and (directly) from the secondary PCI bus to allow the TriMedia to transfer data to each other at full PCI bandwidth. All programs to be run in a TriMedia processor must reside in that processor's local SDRAM.

TriMedia processors have built-in Audio Input and Output interfaces. These synchronous serial ports were intended for stereo digital audio processing, but can be used as general purpose block DMA devices. A loop connection is made using these audio input and output ports. This allows a maximum of 400 KB/s of DMA transfer between adjacent TM-1000s without use of the internal PCI bus.

Each TriMedia has a small serial EEPROM, which contains configuration data (not shown in diagram). Additional configuration data must be loaded by the system BIOS (memory base addresses) and by the run-time software. After a power-on or PCI bus reset, each TriMedia loads clock and ID parameters from the EEPROM. It then stays in a reset state waiting for the host to finish configuration. Since the DSP CPU will not run until the Host completes the configuration process, individual TriMedia may be run stand-alone for debug or test. The DSP CPU reads all instructions from the local SDRAM. After a reset, it begins operation starting at the first location in SDRAM. Thus the host is required to load code into each SDRAM before releasing the reset state of the DSP CPU. Standard PCI and "Plug and Play" requires the host CPU to assign address bases and other parameters at start-up.

## **2. Video Data Paths**

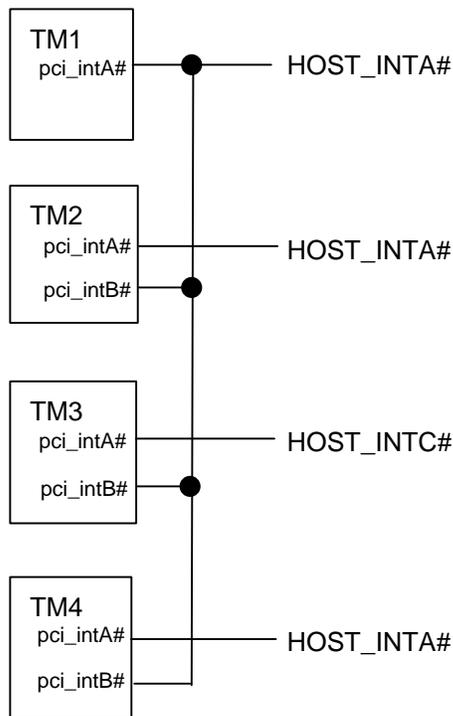
All TriMedia receive video input from the crosspoint switch, and send video output back to the crosspoint switch.

Each TriMedia has byte-wide video input and output ports. TriMedia video input ports accept ITU-R BT.656 (formerly CCIR656) encoded 8-bit color data as well as 8- and 10-bit raw data (with sign or zero extend to 16-bits for 10-bit input). When receiving color data in ITU-R BT.656 mode, the incoming data is automatically broken into three components and stored as separate arrays for Y, Cr, and Cb. The maximum video input clock rate is 38 MHz for ITU-R BT.656 data or up to 80 MHz for raw data. TriMedia video output ports can generate ITU-R BT.656 encoded data streams as well as 8-bit raw data. All video input and output data is passed between the port and the TriMedia local SDRAM.

## **3. Interrupts**

Each of the four TriMedia Processors receives one or two Host interrupt lines from the PCI interface, as diagrammed in Figure 1. Interrupt A in each case is the normal Host interrupt for that processor based on its PCI device address. Interrupt B for TM2 through TM4 receives Host Interrupt A. The TriMedia program can interrupt on its normal interrupt, or can always use Host interrupt A. Note that TM1 must always use its interrupt A line. TM1's interrupt B line is used for the crosspoint JTAG interface.

On the FastImage and FastFrame PMC slots, HOST\_INTA# connects to PCI\_INTA#, B to B, C to C, and D to D. Thus, when a daughter card processor interrupts on PMC interrupt line A, it gets back to the Host on the Host's interrupt line A, and so forth. The FastImage PMC slots have PCI device numbers 8 and 12, respectively.

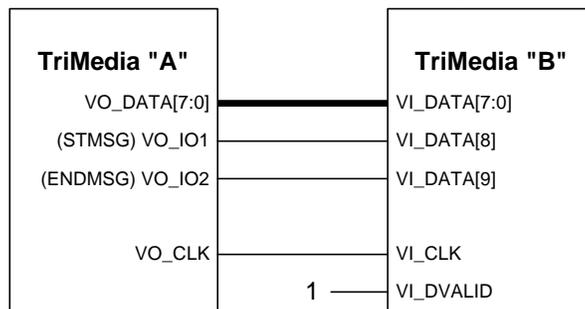


**Figure 3. TriMedia Interrupts**

#### 4. Interprocessor Communication

The FastImage board uses the Video In and Video Out units for interprocessor communication as well as video I/O. A special “message passing” mode allows video outputs to connect to video inputs using 8 data bits along with start and stop message bits (Figure 4). In “message passing” mode, the Video Out unit can pass data to a Video In unit at up to 80 MB/s.

The Video Out unit has a programmable clock generator which can be programmed for byte rates of 4 to 80 MHz. Thus interprocessor link byte rates can be tuned to optimize the data highway (TriMedia internal bus) and SDRAM usage.



**Figure 4. Message Passing Connections**

Video out/in ports not in use for I/O can tie to other TriMedia processors via the crosspoint switch to form a pipeline using “message passing” mode. This allows DMA data transfer between connected processors at 80 megabytes per second without use of the PCI bus. Independent video input and output modules in the TriMedia allow these data transfers to occur in parallel with DSP CPU operations. Simultaneous DMA transfers can also occur between processors over the secondary PCI bus.

## **B. Digital Crosspoint Switch**

The IQX160 digital crosspoint switch is a 160-port non-blocking switch matrix with flexible I/O buffers at each port. The single-bit ports allow the maximum flexibility of interconnection including one-to-many and many-to-one modes. The I/O buffers resemble the I/O macrocells of a gate array or CPLD. The switch matrix is capable of connecting any I/O port to any other I/O port on the device.

Configuration of the switch matrix and I/O buffers is SRAM-based, allowing reconfiguration in system. Configuration data is downloaded to the part via a standard JTAG port. Unlike the FastImage and FastFrame, the Fast4/1300 has no “CPLD” for downloading the crosspoint switch. The crosspoint switch JTAG pins are directly driven by I/O pins of the primary TriMedia processor, TM1.

The TriMedia SSI\_IO2 line drives the active low TRST# input of the crosspoint switch. A low logic level on this line resets the crosspoint switch to its power-on state. On reset all I/Os are set as inputs, all switch matrix connections are broken, and the JTAG state logic is reset. This line should be pulsed low before loading a new configuration to the crosspoint switch.

TriMedia interrupt lines PCI\_INTB#, PCI\_INTC#, and PCI\_INTD# drive the TDI, TCK and TMS inputs of the crosspoint switch respectively. TCK is the JTAG clock line. The crosspoint switch samples TDI and TMS on the rising edge of TCK. Data sequences for TDI and TMS are generated by the I-Cube IDS-100 software package.

The crosspoint's TDO line drives the TriMedia SSI\_IO1 input. Data shifts out from the crosspoint switch at the falling edge of TCK.

The minimum high or low time of TCK is 20 nanoseconds and its maximum allowable frequency is 20 MHz. TMS and TDI must be valid for at least 4 nanoseconds before the rising edge of TCK. TDO is valid at most 15 nanoseconds after the falling edge of TCK.

## **C. PCI-PCI Bridge**

A PCI-PCI bridge chip isolates on-board components from the host PCI bus while allowing a transparent data path between the host and on-board secondary PCI buses. This chip conforms to the PCI specification for bridges and is supported by most BIOSs.

While the bridge chip presents a single electrical load to the host PCI bus, the four TriMedia processors look like four devices to the host system BIOS. The PCI standard allows each device behind a bridge to have its own configuration space, and the PCI BIOS code sets up these devices individually.

## **D. Power**

The Fast4/1300 is built primarily with 3.3 volt and 2.5 volt components. However the only input power required is at 5 volts. An on-board switching DC-DC converter generates the 2.5 volts for the TriMedia cores, and a linear regulator provides the 3.3V for the TriMedia I/O and the SDRAMs.

Because the power requirements of the Fast4/1300 exceed the allowable power for a PMC module, there is an auxiliary connector to supply additional current at 5 volts using an adapter cable. This adapter cable plugs into a standard disk power connector of the PC.

### III. CONNECTOR

#### A. PMC (Pn1, Pn2, Pn4)

The Fast4/1300 card communicates with the main board via PMC connectors (Pn1, Pn2 and Pn4). Pn1 & Pn2 have the standard PCI functions and pinout. Pn4 has 32-bits of FastChannel Digital input/output, 8-bits of control, 4 clocks, and I<sup>2</sup>C. Table 1 shows the pinout.

Pin	PN4 Signal	Pin	PN4 Signal
1	DIG_DO0	33	DIG_DO26
2	DIG_DO1	34	DIG_DO27
3	DIG_DO2	35	GND
4	DIG_DO3	36	DIG_DO28
5	GND	37	DIG_DO29
6	DIG_DO4	39	DIG_DO30
7	DIG_DO5	39	DIG_DO31
8	DIG_DO6	40	GND
9	DIG_DO7	41	DIG_CO0
10	GND	42	DIG_CO1
11	DIG_DO8	43	DIG_CO2
12	DIG_DO9	44	DIG_CO3
13	DIG_DO10	45	+3V_PMC
14	DIG_DO11	46	DIG_CO4
15	+3V_PMC	47	DIG_CO5
16	DIG_DO12	48	DIG_CO6
17	DIG_DO13	49	DIG_CO7
18	DIG_DO14	50	GND
19	DIG_DO15	51	DO_PXCK1
20	GND	52	DO_PXCK2
21	DIG_DO16	53	DO_PXCK3
22	DIG_DO17	54	DO_PXCK4
23	DIG_DO18	55	GND
24	DIG_DO19	56	PMC1_SCL
25	GND	57	PMC1_SDA
26	DIG_DO20	58	PMC2_SCL
27	DIG_DO21	59	PMC2_SDA
28	DIG_DO22	60	+3V_PMC
29	DIG_DO23	61	PMC3_SCL
30	+3V_PMC	62	PMC3_SDA
31	DIG_DO24	63	PMC4_SCL
32	DIG_DO25	64	PMC4_SDA

**Table 1. PMC-Pn4 “FastChannel” Connector**

## **IV. SPECIFICATIONS**

### **A. Processors**

- Full computational power of one to four TriMedia TM1300 VLIW media processors (~ 3.6GOPS) applied to the video streams
- 32 or 64 MB of distributed SDRAM (8 or 16 MB per processor)
- 2.3 GB/s (4 x 571 MB/s) local memory bandwidth
- Memory-mapped host access to distributed SDRAM for bootstrap and program load
- All on-board and host PCI resources can be directly addressed by each processor

Clock rate	180 MHz (200 MHz also available)
Memory	8 or 16 MB SDRAM per processor at 143 MHz (133 MHz memory with 166 MHz processors), 571 MB/s peak access rate at 143 MHz (effective instruction access rate is higher due to compression)
Instruction Cache	32K on-chip cache per processor, 8-way set-associative, 3928 MB/s peak access rate
Data Cache	16K on-chip cache per processor, 8-way set-associative, 1144 MB/s peak access rate

## V. TROUBLESHOOTING

There are several things you can try before you call Alacron Technical Support for help.

- \_\_\_\_\_ Make sure the computer is plugged in. Make sure the power source is on.
- \_\_\_\_\_ Go back over the hardware installation to make sure you didn't miss a page or a section.
- \_\_\_\_\_ Go back over the software installation to make sure you have installed all necessary software.
- \_\_\_\_\_ Run the Installation User Test to verify correct installation of both hardware and software.
- \_\_\_\_\_ Run the user-diagnostics test for your main board to make sure it's working properly.
- \_\_\_\_\_ Insert the Alacron CD-ROM and check the various Release Notes to see if there is any information relevant to the problem you are experiencing.

The release notes are available in the directory: **\usr\alacron\alinfo**

- \_\_\_\_\_ Compile and run the example programs found in the directory:  
**\usr\alacron\src\examples**
- \_\_\_\_\_ Find the appropriate section of the Programmer's Guide & Reference or the Library User's Manual for the particular library and problem you are experiencing. Go back over the steps in the guide.
- \_\_\_\_\_ Check the programming examples supplied with the runtime software to see if you are using the software according to the examples.
- \_\_\_\_\_ Review the return status from functions and any input arguments.
- \_\_\_\_\_ Simplify the program as much as possible until you can isolate the problem. Turning off any operations not directly related may help isolate the problem.
- \_\_\_\_\_ Finally, first **save your original work**. Then remove any extraneous code that doesn't directly contribute to the problem or failure.

## **VI. ALACRON TECHNICAL SUPPORT**

Alacron offers technical support to any licensed user during the normal business hours of 9 a.m. to 5 p.m. EST. We offer assistance on all aspects of processor board and PMC installation and operation.

### **A. Contacting Technical Support**

To speak with a Technical Support Representative on the telephone, call the number below and ask for Technical Support:

Telephone: **603-891-2750**

If you would rather FAX a written description of the problem, make sure you address the FAX to Technical Support and send it to:

Fax: **603-891-2745**

You can email a description of the problem to [support@alacron.com](mailto:support@alacron.com)

Before you contact technical support have the following information ready:

- \_\_\_\_\_ Serial numbers and hardware revision numbers of all of your boards. This information is written on the invoice that was shipped with your products.
- \_\_\_\_\_ Also, each board has its serial number and revision number written on either in ink or in bar-code form.
- \_\_\_\_\_ The version of the ALRT, ALFAST, or FASTLIB software that you are using.
- \_\_\_\_\_ You can find this information in a file in the directory: **\usr\alfast\alinfo**
- \_\_\_\_\_ The type and version of the host operating system, i.e., Windows 98.
- \_\_\_\_\_ Note the types and numbers of all your software revisions, daughter card libraries, the application library and the compiler
- \_\_\_\_\_ The piece of code that exhibits the problem, if applicable. If you email Alacron the piece of code, our Technical-Support team can try to reproduce the error. It is necessary, though, for all the information listed above to be included, so Technical Support can duplicate your hardware and system environment.

## **B. Returning Products for Repair or Replacements**

Our first concern is that you be pleased with your Alacron products.

If, after trying everything you can do yourself, and after contacting Alacron Technical Support, you feel your hardware or software is not functioning properly, you can return the product to Alacron for service or replacement. Service or replacement may be covered by your warranty, depending upon your warranty.

The first step is to call Alacron and request a "Return Materials Authorization" (RMA) number.

This is the number assigned both to your returning product and to all records of your communications with Technical Support. When an Alacron technician receives your returned hardware or software he will match its RMA number to the on-file information you have given us, so he can solve the problem you've cited.

When calling for an RMA number, please have the following information ready:

- \_\_\_\_\_ Serial numbers and descriptions of product(s) being shipped back
- \_\_\_\_\_ A listing including revision numbers for all software, libraries, applications, daughter cards, etc.
- \_\_\_\_\_ A clear and detailed description of the problem and when it occurs
- \_\_\_\_\_ Exact code that will cause the failure
- \_\_\_\_\_ A description of any environmental condition that can cause the problem

All of this information will be logged into the RMA report so it's there for the technician when your product arrives at Alacron.

Put boards inside their anti-static protective bags. Then pack the product(s) securely in the original shipping materials, if possible, and ship to:

**Alacron Inc.  
71 Spit Brook Road, Suite 200  
Nashua, NH 03060  
USA**

Clearly mark the outside of your package:

**Attention RMA #80XXX**

Remember to include your return address and the name and number of the person who should be contacted if we have questions.

### **C. Reporting Bugs**

We at Alacron are continually improving our products to ensure the success of your projects. In addition to ongoing improvements, every Alacron product is put through extensive and varied testing. Even so, occasionally situations can come up in the fields that were not encountered during our testing at Alacron.

If you encounter a software or hardware problem or anomaly, please contact us immediately for assistance. If a fix is not available right away, often we can devise a work-around that allows you to move forward with your project while we continue to work on the problem you've encountered.

It is important that we are able to reproduce your error in an isolated test case. You can help if you create a stand-alone code module that is isolated from your application and yet clearly demonstrates the anomaly or flaw.

Describe the error that occurs with the particular code module and email the file to us at:

[support@alacron.com](mailto:support@alacron.com)

We will compile and run the module to track down the anomaly you've found.

If you do not have Internet access, or if it is inconvenient for you to get to access, copy the code to a disk, describe the error, and mail the disk to Technical Support at the Alacron address below.

If the code is small enough, you can also:

FAX the code module to us at **603-891-2745**

If you are faxing the code, write everything large and legibly and remember to include your description of the error.

When you are describing a software problem, include revision numbers of all associated software.

For documentation errors, photocopy the passages in question, mark on the page the number and title of the manual, and either FAX or mail the photocopy to Alacron.

Remember to include the name and telephone number of the person we should contact if we have questions.

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