Focused Ion Beam Milling of Semiconductors

An imaging challenge

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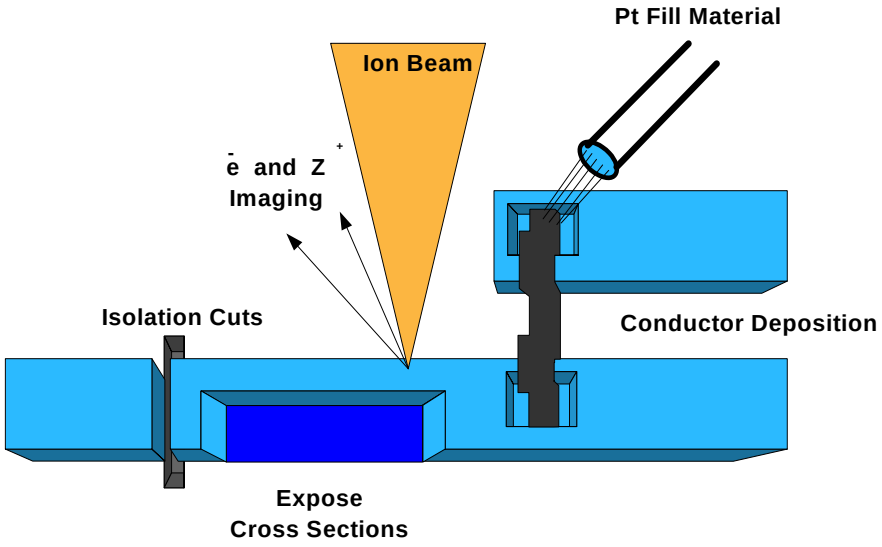
In recent years, the challenges confronting semiconductor engineers have increased exponentially. Not only are new semiconductors harder to design, but also harder to test and debug as a result of growing complexity, decreased feature size, and the introduction of new materials and manufacturing processes. Moreover, in today's environment of continually shortening product life cycles, all of the phases of design, testing, and debugging must be completed on brutally short schedules to prevent the new product from being obsolete when brought to market.

Traditional semiconductor testing and debugging methods, which rely on testing a finished prototype and re-spinning it over and over until it functions as desired as well as increasingly expensive mask sets and other materials can result in substantial added expense and time-to-market delays. The debug stage typically finds both circuit logic errors and potential timing issues. Re-spinning a design to address such issues can cost several months and several million dollars. The best way to avoid such delays and expenses is to insure that errors are detected and corrected in the initial prototype stage by rapidly micro-machining the prototype, thus obviating the need for expensive and time-consuming re-spins.

Focused Ion Beam ("FIB") technology has been the pre-eminent tool for microcircuit editing for almost a decade, and became the preferred microscopy sample preparation tool for site-specific applications. The FIB can both create and modify microstructures. This is accomplished by using the FIB's precision capabilities to (1) remove material, (2) deposit material, and (3) provide localized ion implantation (see below). The FIB also can image the sample via secondary electrons or ions before, after, and during micro milling. The ability to image while removing or depositing material provides important feedback for process control.



Unfortunately, serious drawbacks limit the use of traditional FIB tools to edit circuits. Several days can be required just to drill to the first metal layer. Often companies cannot afford to spend the necessary time trying to perform micro milling on individual transistors and vias. Instead, they skip the circuit-editing step, and simply revise designs, produce new mask sets, run new wafers, and hope for positive outcomes.

The Challenge

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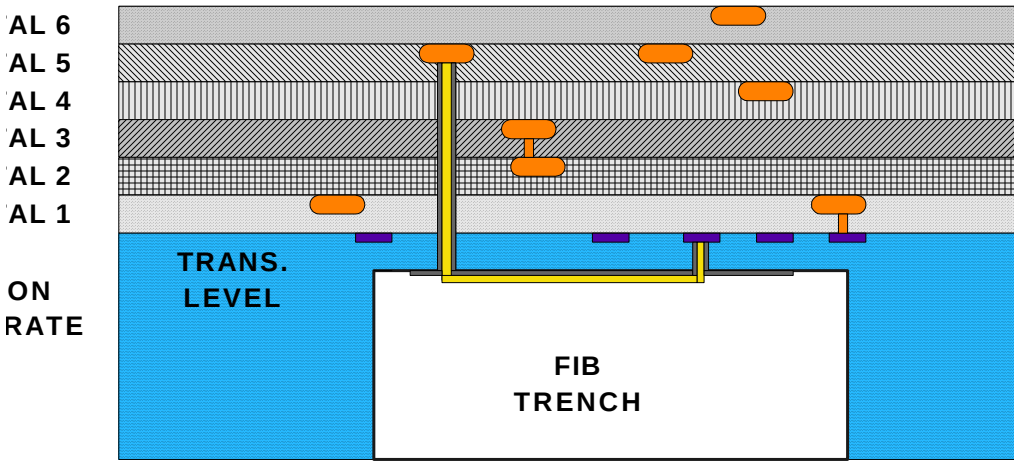
Silicon micro machining consists of modifying a circuit by cutting interconnects in the chip with FIB milling, and forming other interconnects with FIB metal deposition. As diagrammed below, the interconnections are within the active layer of the silicon, sandwiched between the package and bulk silicon. Thus, circuit modification begins with the removal of silicon to access the active layers of the chip, and ends with FIB micro machining.



FIB interconnections commonly are made to metal lines, but must avoid milling transistors or other lines. This restriction places a severe width constraint on the vias made by the FIB. Multiple metal layers incorporating new materials (such as dielectric films and silicon-on-insulator ("SOI"), both of which are sensitive to invasive charged particles) and advanced packaging techniques (such as flip-chip) have severely compounded the problem. At the same time, the width of the gate structure in transistors is rapidly shrinking to less than 0.09 micrometers, thus rendering traditional circuit-editing techniques obsolete. For example, to reach M1 and initiate editing and milling with standard FIB tools, an average time was eight hours, according to NPTest sources.

The principal FIB equipment manufacturing companies, such as FEI, JEOL, NPTest (formerly Schlumberger), Seiko, and LEO, currently are attempting to develop advanced FIB techniques in order to revive the declining FIB tool market. Their goals are to increase FIB accuracy, while significantly decreasing micro-milling time. Accomplishment of those goals would greatly enhance the utility of such advanced FIB devices to semiconductor manufacturers, by allowing them to emulate the results of their editing, i.e. cutting and adding traces, without the time and extreme expense of creating a new mask. The critical issues encountered by FIB equipment companies in developing advanced techniques are discussed below.

A Solution

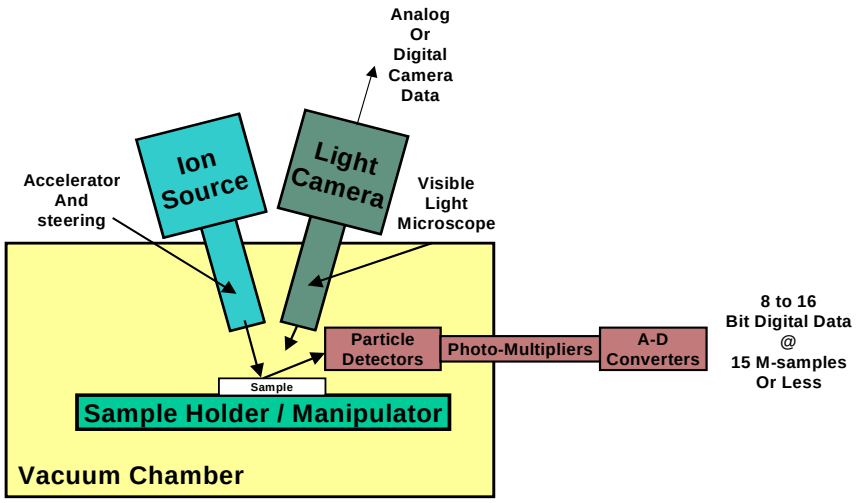
Using the standard FIB approach efficiently in conjunction with the newer semiconductor feature sizes, complexity, and layouts requires achievement of the following goals:

- Precise Beam Placement: In editing a semiconductor device, the crucial step is precise beam placement. Accuracy of placement is even more important than beam size in determining the quality of the outcome. Editing transistors with today's sub nanometer dimensions and high densities leaves little room for error and is time consuming in the extreme.

- Elimination of Semiconductor Movement: Eliminating the need to move the device to image and then machine significantly increases both productivity and accuracy of device editing. Moving a chip back and forth can cause package warp and decreased accuracy in editing.

- Imaging Assured to 0.1 Micron Accuracy: As a result of growing complexity and the introduction of new materials and manufacturing processes. The capability to visually navigate across a device and produce a FIB box assured to 0.1-micron accuracy is necessary to insure accurate and precise editing and deposition.

To achieve these goals, NPTest developed a new FIB device called the IDS OptiFIB, which is diagrammed below. The IDS OptiFIB integrates an optical and ion microscope in a single, coaxial tube that operates simultaneously during circuit analysis and editing following first silicon. This simultaneous ability reduces milling time from hours to minutes.

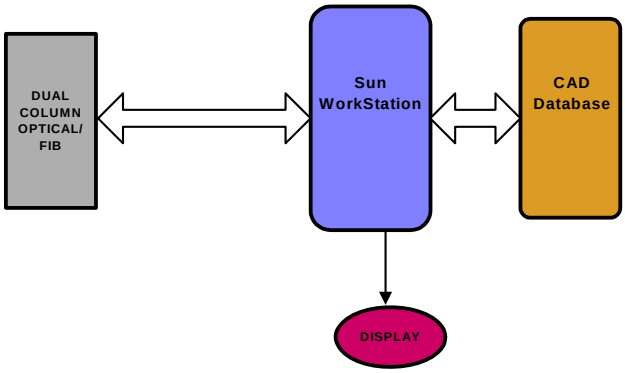


According to NPTest, the OptiFIB can edit from the front or backside of a wafer, regardless of the material used in the IC stack employing the integrated microscopes. The OptiFIB features in-situ alignment, combining ion and photon optical microscopes in a coaxial photon ion microscope to support front-side and backside milling, using through-silicon imaging. Viewing the real-time optical image through silicon during the ion beam editing process accommodates accurate end pointing to stop milling. As a result, the system can perform edits on any manufacturing process technology, including SOI, low-k, and copper. Because the OptiFIB can edit circuits from the front or back side, and its optical microscope provides noninvasive, infrared imaging, it can use optical end pointing during the milling process, skipping several traditional steps in FIB editing, such as creating fiducial trenches. These features also increase throughput and accuracy, because the OptiFIB navigates to the first metal layer in about 30 minutes. The optical imaging can also see through low-k dielectric materials and silicon-on-insulator, as well as silicon, allowing backside editing of circuits. This is because all of a chip's signals are routed through the initial metal layer.

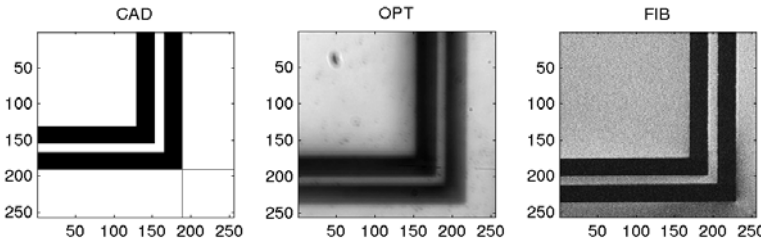
Improved accuracy with optical navigation

The OptiFIB tool allows IC diagnostic engineers to etch and deposit metal while concurrently imaging safely on today's advanced devices. The OptiFIB system uses

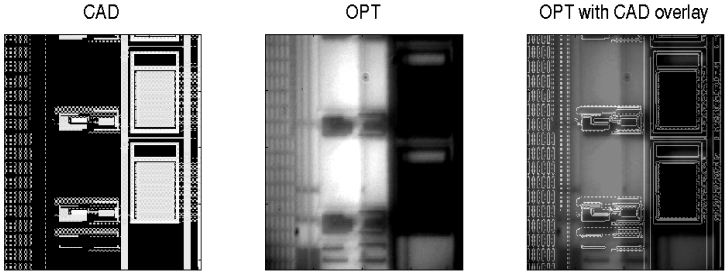
photons to enable non-invasive, through-silicon imaging, resulting in optical images that can be used for accurate navigation. The coaxial column and photon optics enable the user to see through silicon (including dielectrics and heavily doped silicon) to accurately align the FIB and CAD images and simultaneously drill with unparalleled precision. The CAD layout tool enables the user to overlay the CAD with the optical and FIB images ensuring 0.1 micron edit accuracy (see below).



Placement accuracy is achieved by making use of the sub-pixel resolution algorithm typically performed in advanced lithography. This algorithm provides a precise way to align CAD data and the optical image, as demonstrated in the front and back images below.



CAD, IR and FIB images of front side ICfor verifying <100nm placement
189 nm/pixel, 48.38 *m*. FOV

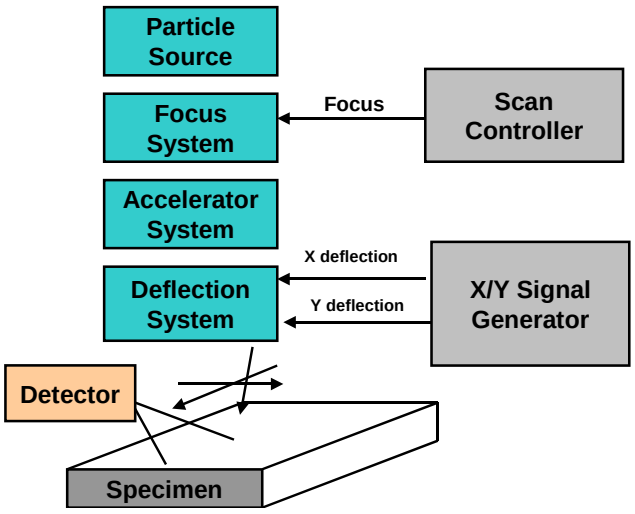


CAD layout and 1064nm optical image (1700*nm* resolution, 360*nm* pixel resolution) of IC inverter output section
Goal to accurately align images for backside probing and editing.

The OptiFIB is easy to align and features achromatic imaging technology to maintain alignment. Achromatic imaging, using a set of mirror lenses instead of glass, eliminates image aberrations when moving from blue to infrared light. This feature of the coaxial column enhances image quality and real-time simultaneous imaging, providing continuous device modification feedback to ensure confidence and editing success. Through-silicon navigation and imaging utilize the capabilities of the newly designed coaxial column. This instrument enables users to optically view editing locations while performing modifications. Further, users can have software-driven, low ion-current end point detection to control the milling depth more accurately. An “End Point Analyzer” detects changes in device material, prompting automated milling termination.

Signal Acquisition Challenges

The position of the FIB beam is determined by the X/Y waveform generator, which can scan it with any path the designer of the system desires. In scanning (SEM and FIB) systems it is normal to restrict the beam path to areas of interest for diagnostic measurements of both secondary electrons and X-Rays for imaging. In FIB systems the path of the beam can be used to remove or add material (as controlled by the focus and energy of the beam) and moves at a non-Cartesian slow rate.



Thus, a FIB system presents several challenges to the data acquisition interface boards. Often these systems use custom interface (e.g., frame grabber) boards to provide the functionality required. Using an off-the-shelf solution demands that the frame grabber have the following two characteristics:

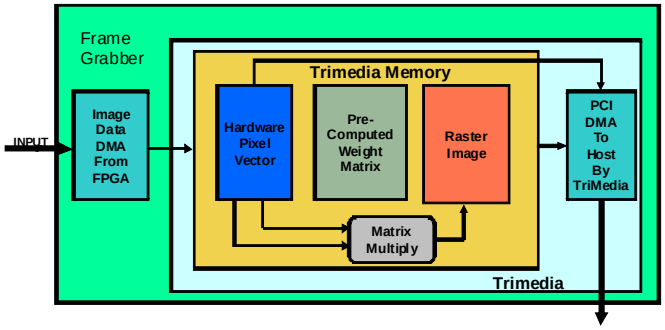
- The range of pixel clock speeds must be extremely large, from 10K to 10 MHz. In order to improve the look and feel of these systems, partial frames must be delivered to the user so that the image can be developed as it’s being scanned.

Normal frame grabbers are “frame oriented”—i.e., the data is provided when the frame is done.

- Both FIB and SEM applications take advantage of the ability of the source to do non-raster scanning. Accordingly, the non-raster-oriented image must be converted to a raster-oriented image for display.

The Alacron’s FastFrame1300, which is pictured below, meets the foregoing requirements. The FastFrame1300 has an input FPGA, which feeds directly into an image processor (the TriMedia TM1300 microprocessor from Philips Semiconductors) that can be used to reformat the data.

More specifically, pixel values flow from the hardware in the order in which they are scanned. The pixel locations are provided to the frame grabber as x/y coordinates, which are not aligned to the desired raster pixels. The framer grabber software, which is diagrammed below, pre-computes a table that defines which pixels in the hardware data are used to compute the values of each pixel in the raster image. In other words, the raster image is derived from the hardware image. The raster pixels are weighted sums of the hardware pixels. The weights for a raster pixel are computed from the values of the four nearest hardware pixels, above, below, and left and right of the raster pixel location. The actual conversion is done using the on-board TriMedia processor, on the hardware pixels, and the raster and vector images are sent to the host. The raster image is displayed for the user, and the hardware image is used to control the system (focus, energy, etc. depending on the application).



As discussed above, image quality is an important requirement for the accuracy of a circuit-editing machine in the world of 90 nm processes. The Alacron FastFrame1300, with its flexible FPGA/CPU architecture, enables the production of enhanced images in real-time, enabling NPTest to produce a state-of the-art FIB tool with an off-the-shelf frame grabber

Conclusion

The increased accuracy and utility of the OptiFIB could save a semiconductor design company an entire debug/fabrication cycle, avoiding additional expenses of $1-2 million and several weeks of delay. The other FIB toolmakers are at the same time pursuing their approach to the same goal and are introducing new designs. The results of such competition can produce significant benefits for the suppliers, customers, and ultimately consumers.