Application Paper

Industrial Inspection Imaging Application

As an example of the performance of Alacron's heterogeneous image processing platform, an industrial inspection imaging application implemented on Alacron's heterogeneous C80 / multiprocessor SHARC environment is illustrated, and compared with implementations using the C80 and SHARCs alone.

A product is examined as it moves rapidly on a production line, and rejecting it if it is found to be defective. A digital camera generates 512 pixel x 512 line 24 bit red-green-blue (RGB) images at 30 frames / second. These images are converted to hue-saturation-lightness (HSL), and filtered. Pixels of like color are combined into regions, and statistics on the regions are gathered and processed by a neural network classifier to determine if the product is defective. To keep up with the production line, this application must be able to perform continuously at a 30 per second frame rate. The steps in the application are shown in Table 1, along with required processing times.

Step	Function	Platform Location	Time (ms)
1	Read image from Video Interface	C80	3.9
2	LUT translation of Image Colors	C80	2.0
3	RGB to HLS color Space Conversion	C80	5.2
4	Filtering of the Image	C80	14.0
5	DMA Transfer to Global DRAM	-	3.9
6	Transfer Image into SHARC Array	SHARC	4.9
7	Fix to Float of color pixels	SHARC	2.5
8	Color Sobel Filtering (Edged Detection)	SHARC	8.2
9	Region Labeling and Sizing	SHARC	9.0
10	Neural Network Evaluation	SHARC	0.3
11	Defect Decision and Signaling	SHARC	1.0
12	Display of defective image	C80	2.0

Table 1: Implementation on heterogeneous C80 / SHARC platform

In the heterogeneous environment, the C80 section of the system reads the image from the video interface, performs color space conversion and initial filtering. The resulting image is then placed in SDRAM, and the DMA engine transfers it to global DRAM. An 8 processor SHARC array then takes the image from global DRAM, determines the regions of common color using a color version of a Sobel filter, determines the size of each region in pixels, passes the resulting features to a neural network based classifier, which determines if the product is defective. All of the DMA transfers occur in parallel with computation.

The first step is reading the image from the video interface. The video interface supplies packed data to the C80 at 200 MB/s. When the FIFO signals the C80 that it is almost full, the C80 reads the image data out of the FIFO and processes it. The C80 processes each block of data as it comes in, keeping up with the flow of image data, and processing it in parallel with the refilling of the FIFO with more image data. The whole image takes 768 K bytes of data (512*512*3) which takes 3.9 milliseconds transferring at 200 MB/s.

LUT translation of the image colors takes 1 clock for each of the three bytes in each pixel. Each PP in the C80 processes 2 bytes of each pixel in the input image. The 4 PP together can process pixels at 400 million pixels per second. The LUT step of the processing thus takes 512*512*3 / 400,000,000 or 2.0 milliseconds.

The RGB to HLS conversion is performed in two steps. First, the lightness component is computed, L = (R+G+B)/3. This requires 2 clocks. The remaining part of the conversion requires 6 clocks for a total of 8 clocks per pixel. Each PP can process two pixels at a time, so 8 pixels can be processed at the same time. This entire process takes 512*512*8 / 8 / 50,000,000 or 5.2 milliseconds.

The final filtering step takes 10 clocks per pixel, which when divided across the 4 PP processors, gives 13.1 milliseconds, or 14.0 milliseconds considering overhead in the filter routine.

Following filtering, the DMA controller in the SHARC array transfers the image from global DRAM into the local dual ported memory accessible by the individual processors. At 160 MB/sec, this operation takes 512*512*3 / 160,000,000 or 4.9 milliseconds. The DMA controller automatically divides the image into 8 parts, duplicating rows as necessary. Pixel values are then converted to floating point. Each SHARC processes 1/8 of the image and floats each byte in one clock, or 512*512*3/8/40,000,000 seconds or 2.5 milliseconds.

The color Sobel filtering step takes the lightness and hue values for each pixel and performs an edge detection step by comparing pixels across a two by two cell. This step requires 10 clocks per pixel, and each processor processes one eighth of the image or 8.2 milliseconds. Region detection and statistic generation are performed by each processor operating on its part of the image, followed by a final merge step by one processor. When regions overlap the image boundaries between processors, the final merge step detects the overlap and combines the totals for those regions. This step takes approximately 11 clocks, or 9 milliseconds, per pixel.

The neural network evaluation step is performed using a previously trained 4 layer back propagation network with 200 input nodes, 200 hidden nodes in the first hidden layer connected to 50 nodes in the second hidden layer, and 4 output nodes in the output layer. The 4 output nodes indicate reject, marginal conditions, shut down, and acceptable. If the acceptable output is below one half, the product is rejected. This step involves a 200 x 200 matrix multiply, a 200 x 50 matrix multiply, and a 50 x 4 matrix multiply. Additionally, 254 sigmoid function calls are made. This process takes 300 microsecond when split across the 8 processors in the SHARC array.

If the product is then rejected, the image is moved to the VGA display by the C80, and the control processor signals the host system. These steps take approximately 2 and 1 millisecond respectively.

The total of the times for steps 1 to 5 is 29 milliseconds, thus the C80 section of the system is able to keep up with the required 30 Hz frame rate (33 Milliseconds per frame). Similarly, the total times for steps 5 to 11 is 29.8 milliseconds, and therefore the eight processor SHARC array is also able to keep up with the 30 Hz frame rate. Since C80 and SHARC sections operate concurrently on data from sequential frames, the entire system is able to keep up.

Implementation on Homogenous Systems

While this application could be implemented on homogenous processor systems based on C80s or SHARCs alone, the cost and complexity of such designs would be significantly greater.

Using a C80 system alone would require that most floating point algorithms performed by the SHARCs in the heterogeneous solution now be performed in fixed point, with the exception of limited tasks able to be accommodated by the C80's MP core. Even if the associated numerical compromises were acceptable, three additional C80 processors would be required to keep up with the 30 Hz frame rate.

Similarly, a homogenous SHARC solution would require eight additional SHARC processors to keep up. Furthermore, since the C80 processor itself supplies support for video input and output operations that is not provided by the SHARC, a "SHARC only" solution would require a separate framegrabber interface and video display interface.

In both cases, the need for additional processors and hardware interfaces would increase the cost of the homogeneous solutions by a factor of two over Alacron's heterogeneous solution. This real-world application is very costly when implemented using homogenous C80 or SHARC solutions, but becomes substantially more cost-effective on Alacron's heterogeneous imaging platform using a C80 combined with an array of eight SHARC processors.

Conclusion

A heterogeneous solution can be the best solution for complex imaging applications that are suboptimally or inefficiently performed in homogenous fixed or floating point environments.

Alacron provides FT-C80 and FT-SHARC boards for integer and floating point intensive real-world imaging and DSP application on VME, ISA and PCI bus hosts, as well as processor daughter cards which enable heterogeneous solutions, such as the one illustrated here.

FT-C80 boards support a range of tightly coupled on-board digital and analog frame-grabbers, as well as video output. Both FT-C80 and FT-SHARC support a wide range of interchangeable I/O expansion boards, including analog and digital framegrabbers, high performance digital I/O interfaces, SCSI and VSB, and a high resolution video display adapter.

Alacron's high performance subsystems provide excellent choices for demanding memory and I/O intensive real word imaging and DSP applications.

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