Technical Paper

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The Impact of Future Microprocessors on Imaging Technology

Imaging systems employed in demanding industrial and military applications, such as computer vision and automatic target recognition, typically require real-time high-performance computing resources. While these systems have traditionally relied on proprietary architectures and custom components, recent advances in high-performance microprocessor technology have produced an abundance of low cost components suitable for use in high-performance computing systems.

A common pitfall in the design of high-performance imaging systems, particularly systems employing scalable multiprocessor architectures, is the failure to balance computational and memory bandwidth with I/O. The recent introduction of microprocessors with large internal caches and high-performance external memory interfaces make it practical to design high-performance imaging systems with balanced computational and memory bandwidth. In these systems, both the board level memory and I/O architecture, as well as the microprocessor memory, have significant performance impact. Systems that do not scale the memory bus bandwidth as processors are added do not improve in performance, or they reach a limiting value after some initial small gains in performance. In addition, the I/O bandwidth plays a significant role in overall performance.

Therefore, the most important factors in the selection of a programmable imaging system are: (a) will the system be "native" or will it use a co-processor model, (b) which processor has the correct balance of processing and I/O for the application, and finally (c) what is the overall cost? Real-world examples of such designs will be presented, and their performance and cost will be analyzed.

Description of the Application

In order to characterize the advantages of the various state-of-the-art microprocessors, we will calculate the performance of the latest microprocessors from Analog Devices, Intel, Philips Semiconductors and Texas Instruments[1].

The important properties of the selected processors are presented in the following table. Cluster mode designs will reach bus saturation very quickly, to the point that adding additional processors will not improve the rate at which calculations can be performed. The table assumes that the processors are isolated from each other when they are performing the calculations. This assumption is made because most multiprocessor co-processor boards have isolated or local memory designs due to scalability issues. The only non-local memory design is the "native" PIII-450 design, which is added for comparison purposes.

SPECIFICATION	Intel PIII-450	Philips TM1300	TI C6701	ADI 21160
Architecture	CISC	VLIW	VLIW	VLIW
FPU	Yes	Yes	Yes	yes
MFLOPs (Peak)	250	720	1000	600
MIPS (Peak)	450	900	1336	100
MOPS (Peak)	900	4860	1336	800
Memory Bus Bandwidth (MB/s)	800	572	332	400
1K FP cfft (µsec)	300	106	108	90
1K 16 bit cfft (µsec)	191	63	108	90
1K FP dot product (µsec)	7.38	2.84	3.07	5.12
16x16 MACs (MMAC/s)	2.32	1.42	3.07	5.32
8x8 MACs (MMAC/s)	9.34	6.55	7.11	11.80
512^2x8 bit Conv3x3 (msec)	5.34	2.62	7.11	11.80
512^3x8 bit Erosion/Dilation (msec)	7.34	1.42	3.62	3.93
"Glue" Logic Cost ($/CPU)	$150	$3	$65	$39
CPU Price ($)	$300	$100	$150	$100

The Large Data Set Application

Inspection of a large area was modeled for the Philips TM1300, the Analog Devices ADSP21160, the TI TMS320C6701 and the Intel Pentium III-450. The image size is 4096 x 32768 8 bit pixels, or 134.2 Mbytes. Four 1K line scan cameras, each operating a 12.5 MHz, supplied data to the system at 50 mega-pixels per second. The processors perform a total of 7.65 giga-floating-point-operations to process the image. During processing, the processors accessed an external copy of a portion of the image 5 times. The algorithm produces 10 Mbytes of result data per image. A summary of the operations per pixel is shown in the table below.

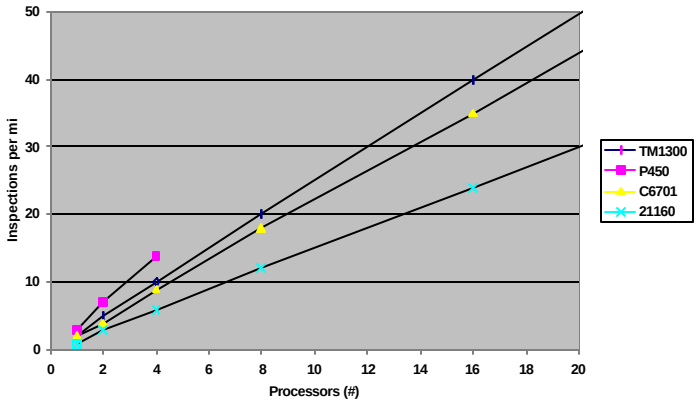
[1] The Motorola PPC750-AV (AltiVec) and the Hitachi/Equator MAP1000 are not presented since, at the time of this writing, there is not sufficient public information available to adequately present them.

2 & 3 Herman, GT. "Image reconstruction for projections", Academic Press. 1980.

Function	Byte Reads	Byte Writes	fmult	fadd/fsub	fcomp	Float	Fix
Fix to Float	1					1	
3x3 conv		4	9	8			
Sobel	4		18	17	2		
Threshold					1		
Store ans		1					1
Total	5	5	27	25	3	1	1

The performance of the processors is expressed in images processed per minute in the table below. The Intel Pentium III-450 gives the best performance, as the processing is substantially memory limited, and the Pentium has the highest performance data bus (800 MB/s). The next best performing processor is the TM1300. The TM1300 supplies the lowest-cost solution for a given level of performance and runs about 73% of the Pentium III, but is about one quarter the cost. The TM1300 has the next higher bus performance of the four processors (584 MB/s).

	Frames Per Minute							
# Processors >>	1	2	4	8	16	32	64	128
TM1300	2	5	10	20	40	79	158	316
P450	3	7	14					
C6701	2	4	9	18	35	71	142	284
21160	1	3	6	12	24	48	96	192



The Real Time Imaging Application

A real time imaging application in which a 512 x 512 eight bit per pixel image is collected at 30 frames per second. The images are inspected for defects. This application required the processors to access an external copy of each frame five times, and perform 16 clocks per pixel of internal computation on each image to detect defects. The inspection algorithm included 1 clock for fix-to-float conversion, 6 clocks for a pre-filter, 6 clock for Sobel edge detection, 1 clock for thresholding, and 2 clocks for image evaluation. 16,384 bytes of output per frame were generated. The total operations per pixel is summarized in the following table.

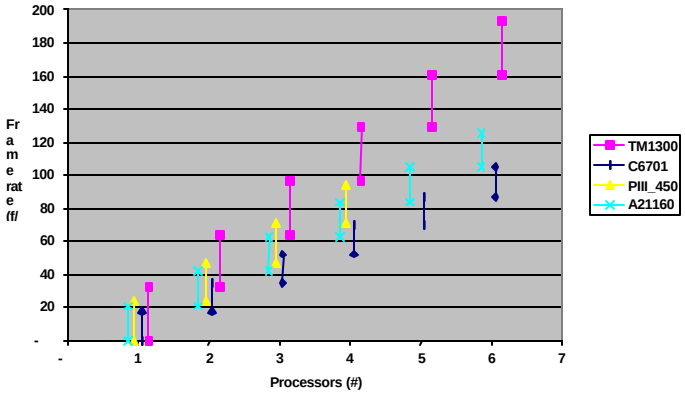
Function	Byte Reads	Byte Writes	fmult	fadd/fsub	fcomp	Float	Fix
Fix to Float	1					1	
3x3 conv		4	9	8			
Sobel	4		18	17	2		
Threshold					1		
Store ans		1					1
Total	5	5	27	25	3	1	1

The table below shows the time it takes each processor to process a frame. A single TM1300 processor can keep up with the frame rate while the other processors require processors to keep up. The compute intensive nature of this application allows the TM1300 to out perform the other processors because of its many arithmetic units. The Pentium III comes close to working because its high performance memory bus compensates for its lower processing throughput.

Number of CPUs by frame rate	Image (msec/fr)	30 fps	60 fps	90 fps	120 fps
TM1300 DSP	24.394	1	2	3	3
P450 CPU	33.204	2	2	3	4
C6701 CPU	45.007	2	3	5	6
21160 CPU	37.355	2	3	4	5

fps = frames per second

The graph below displays the range of frame rates obtainable for each quantity of processors.



Performance of a real time imaging application.

Conclusions

An example application has been presented illustrating how memory bandwidth and processor performance limits the performance of multiprocessor systems. Memory bus saturation severely limits the scalability of cluster based architectures (i.e. PIII-450), while local memory architectures allow throughput to scale linearly with the number of processors.

Notably an excellent DSP processor, the Intel PIII is limited by its surrounding logic (the PC) and is unable to perform in some applications. Although the use of the AGP bus would improve the situation, its SMP design will ultimately limit its scalability. Therefore the most practical solution for demanding application remains a co-processor board that is more scalable, has higher throughput and ultimately is cheaper than the native solution.

The new VLIW processors also provide an advantage over more traditional designs because of the large number of processing elements and issue slots. These architectures perform well even when compared to processors at five times their clock speed.

*Correspondence: Email; joe@alacron.com; http://www.alacron.com; Fax (603) 891-2750

71 Spit Brook Road, Suite 200
Nashua, NH 03060
Tel: 603.891.2750 Fax: 603.891.2745
Web: www.alacron.com E-mail: sales@alacron.com